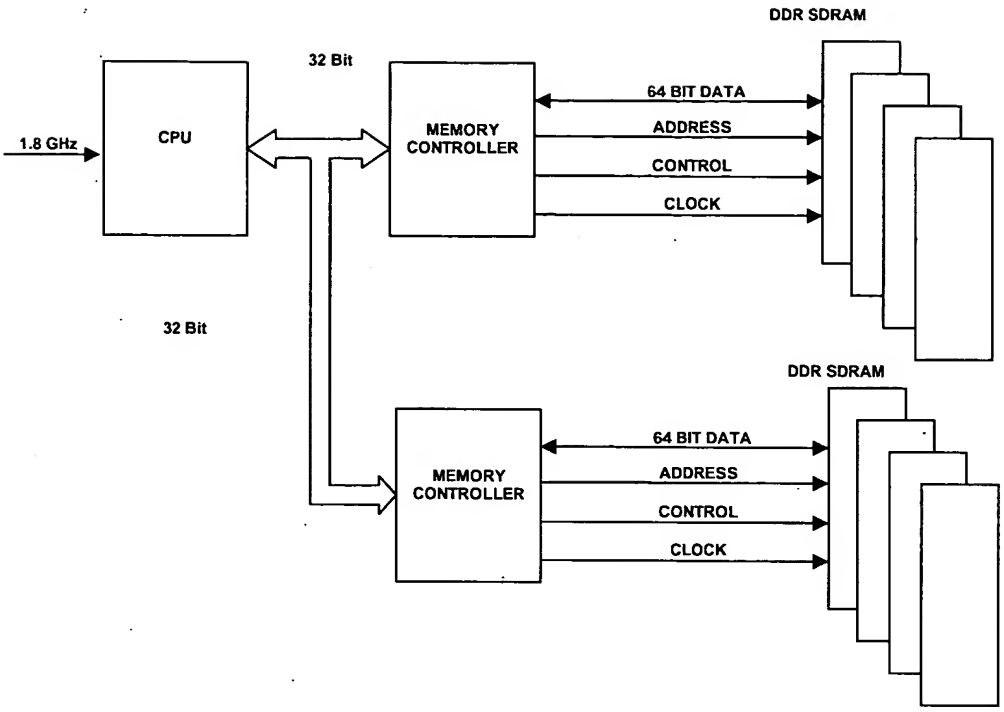

FIGURE 1

(Prior Art)

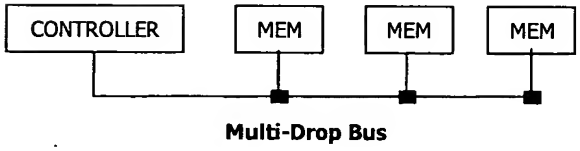

FIGURE 2

(Prior Art)

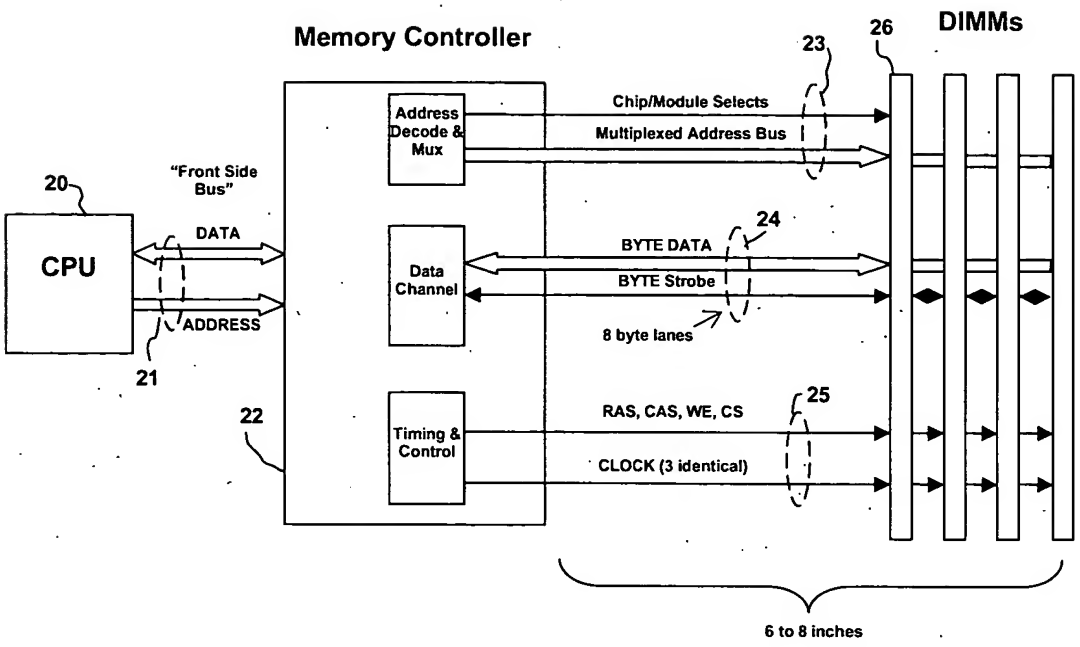

FIGURE 3

(Prior Art)

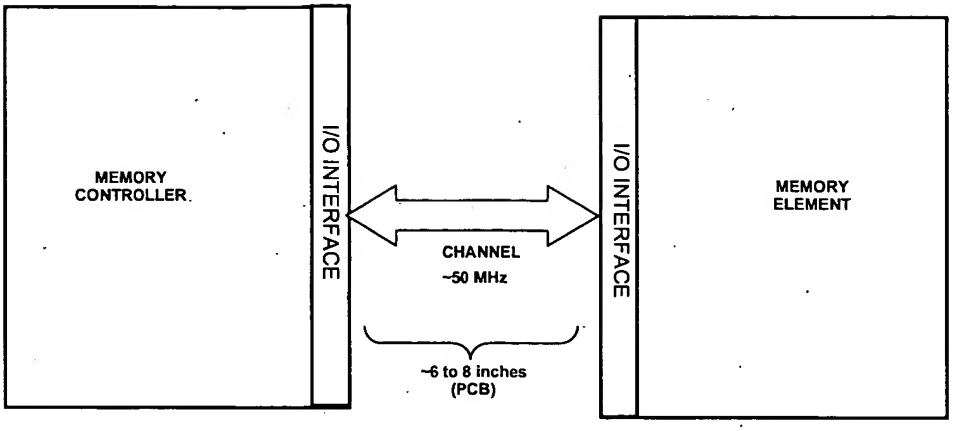

FIGURE 4

(Prior Art)

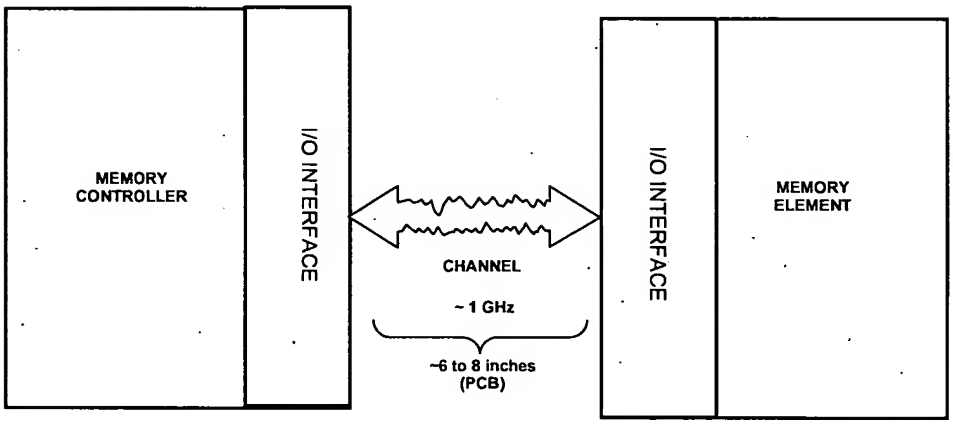

FIGURE 5

(Prior Art)

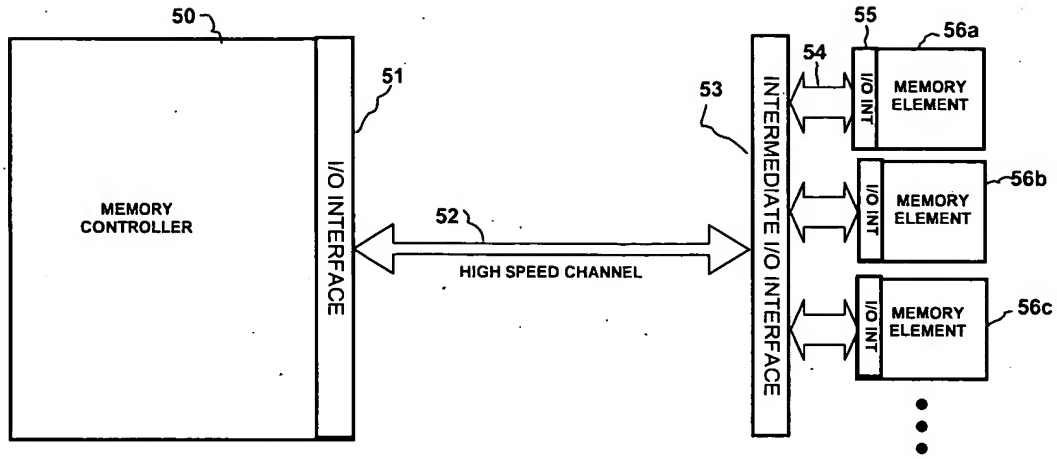

FIGURE 6

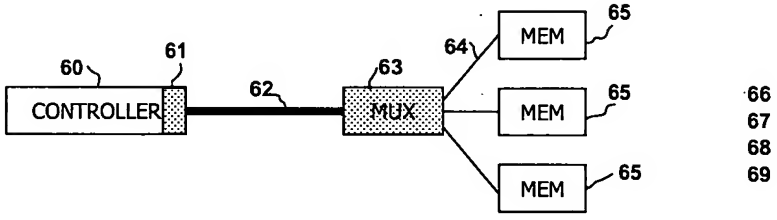

FIGURE 7

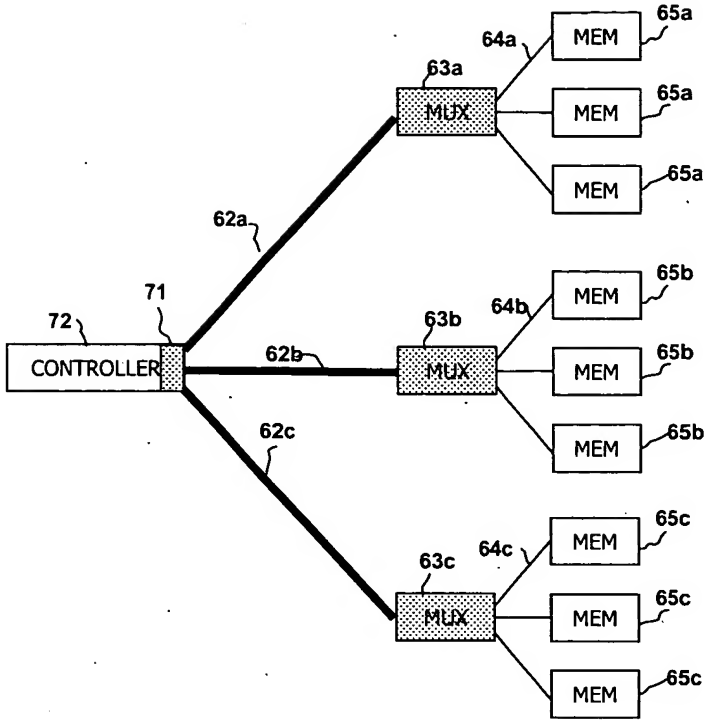

FIGURE 8

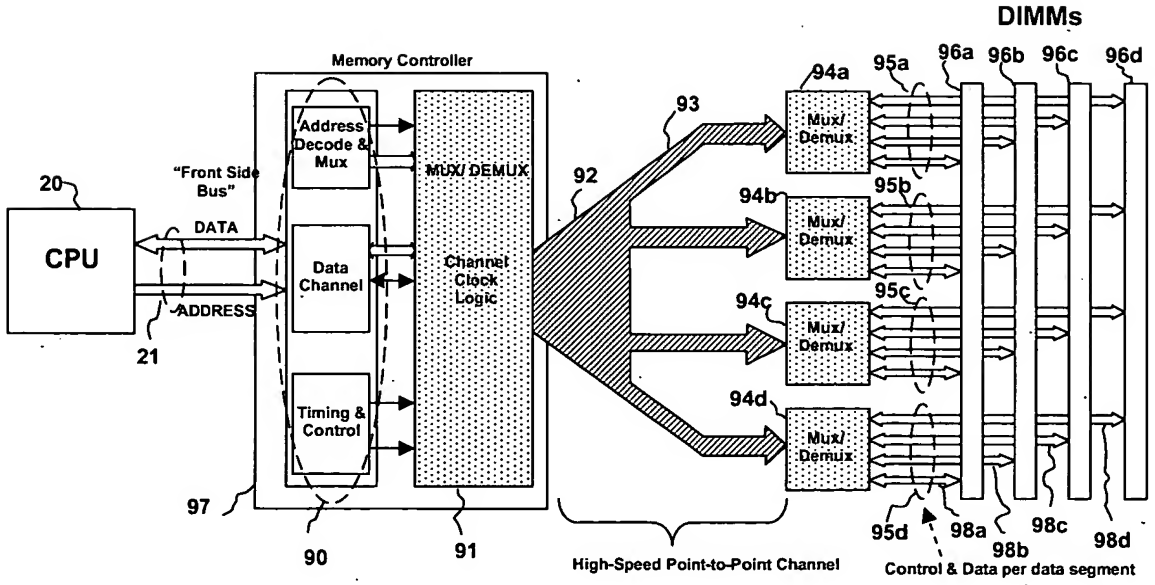

FIGURE 9

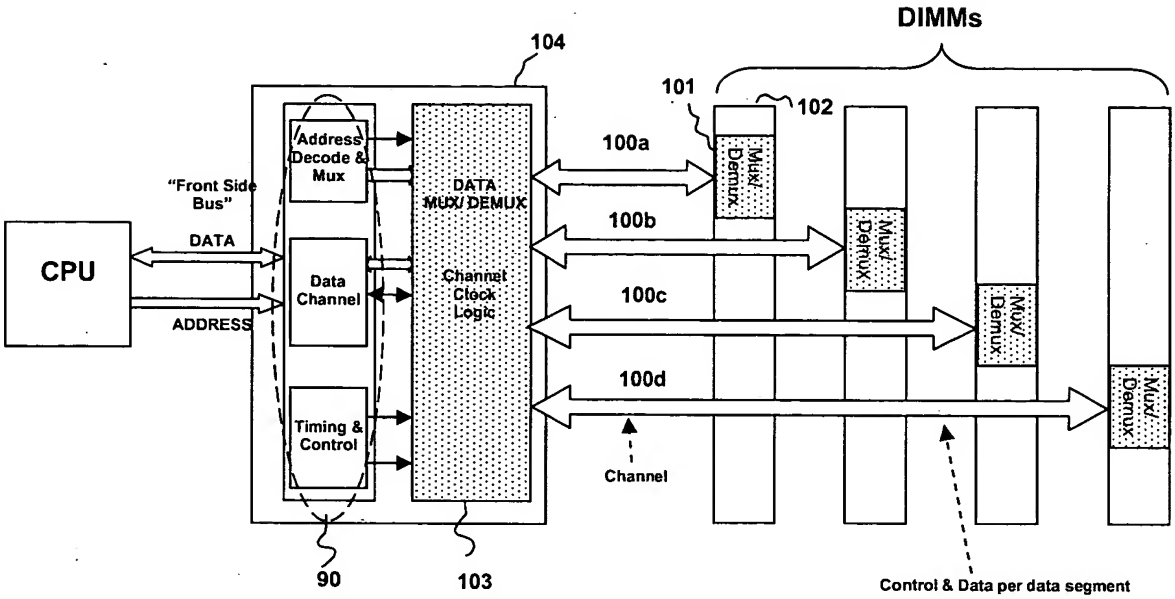
DIMMs
104
101
102
100a
100b
100c
100d
"Front Side Bus"
DATA
ADDRESS
CPU
Address Decode & Mux
Data Channel
Timing & Control
DATA MUX/ DEMUX
Channel Clock Logic
Mux/ Demux
Channel
90
103
Control & Data per data segment

FIGURE 10

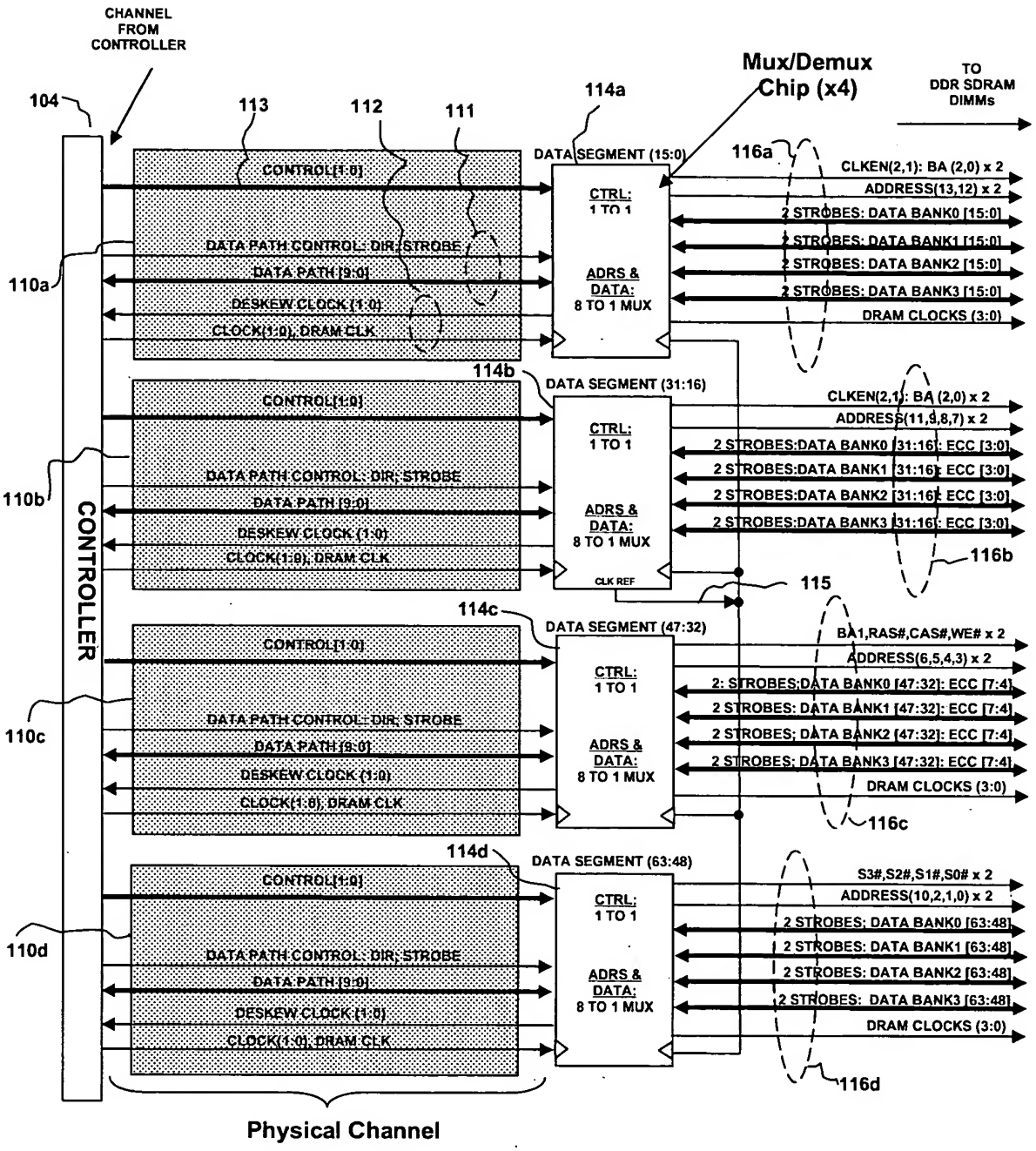
CHANNEL FROM CONTROLLER
104
113
112
111
114a
Mux/Demux Chip (x4)
TO DDR SDRAM DIMMs
DATA SEGMENT (15:0)
116a
CONTROL[1:0]
DATA PATH CONTROL: DIR; STROBE
DATA PATH [9:0]
DESKEW CLOCK (1:0)
CLOCK(1:0), DRAM CLK
CTRL: 1 TO 1
ADRS & DATA: 8 TO 1 MUX
CLKEN(2,1): BA (2,0) x 2
ADDRESS(13,12) x 2
2 STROBES: DATA BANK0 [15:0]
2 STROBES: DATA BANK1 [15:0]
2 STROBES: DATA BANK2 [15:0]
2 STROBES: DATA BANK3 [15:0]
DRAM CLOCKS (3:0)
110a
114b
DATA SEGMENT (31:16)
CLKEN(2,1): BA (2,0) x 2
ADDRESS(11,9,8,7) x 2
2 STROBES:DATA BANK0 [31:16]: ECC [3:0]
2 STROBES:DATA BANK1 [31:16]: ECC [3:0]
2 STROBES:DATA BANK2 [31:16]: ECC [3:0]
2 STROBES:DATA BANK3 [31:16]: ECC [3:0]
116b
110b
CONTROLLER
CLK REF
115
114c
DATA SEGMENT (47:32)
BA1,RAS#,CAS#,WE# x 2
ADDRESS(6,5,4,3) x 2
2: STROBES:DATA BANK0 [47:32]: ECC [7:4]
2 STROBES: DATA BANK1 [47:32]: ECC [7:4]
2 STROBES; DATA BANK2 [47:32]: ECC [7:4]
2 STROBES; DATA BANK3 [47:32]: ECC [7:4]
DRAM CLOCKS (3:0)
116c
110c
114d
DATA SEGMENT (63:48)
S3#,S2#,S1#,S0# x 2
ADDRESS(10,2,1,0) x 2
2 STROBES; DATA BANK0 [63:48]
2 STROBES: DATA BANK1 [63:48]
2 STROBES: DATA BANK2 [63:48]
2 STROBES: DATA BANK3 [63:48]
DRAM CLOCKS (3:0)
116d
110d
Physical Channel

FIGURE 11

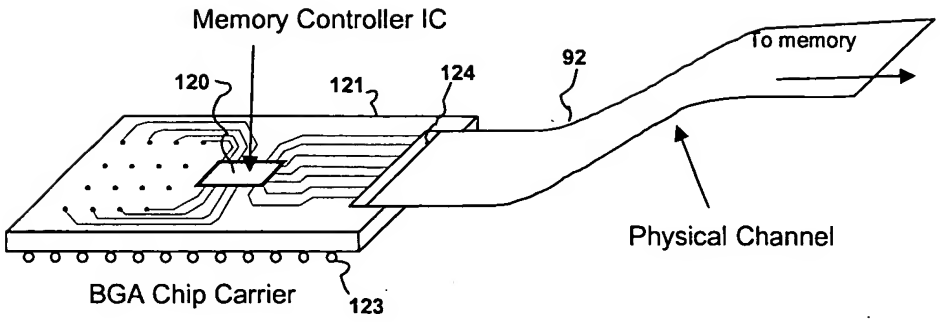

FIGURE 12

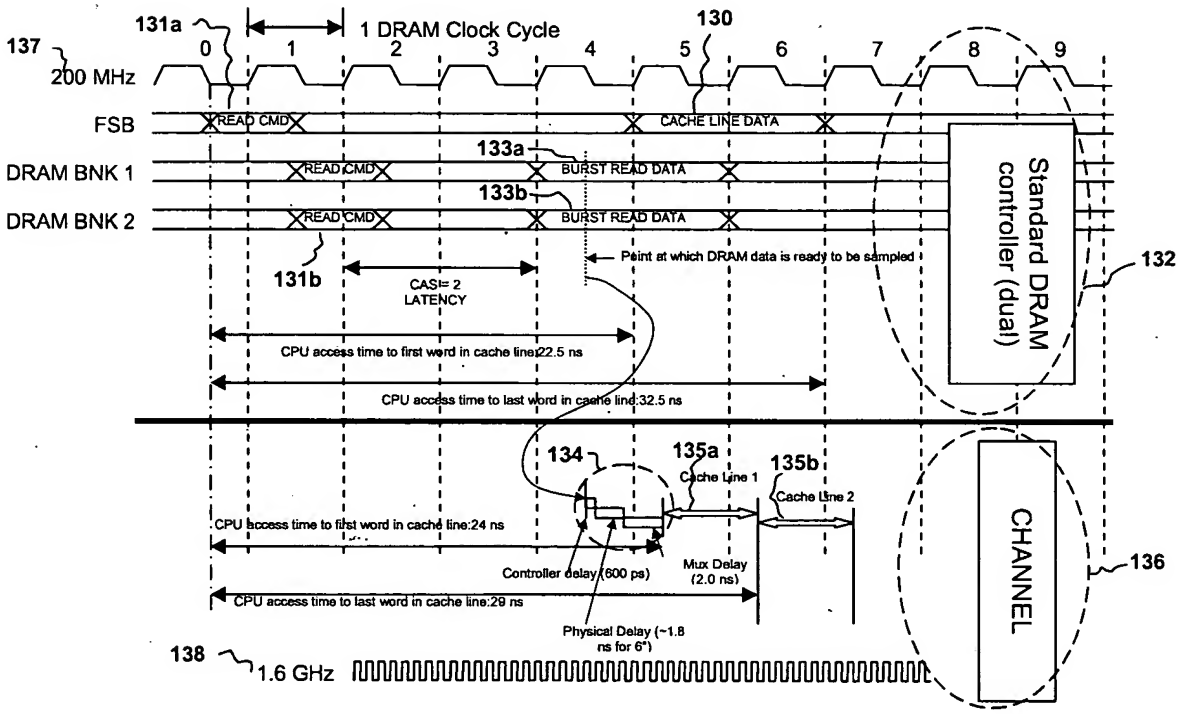

FIGURE 13

FIG. 14A

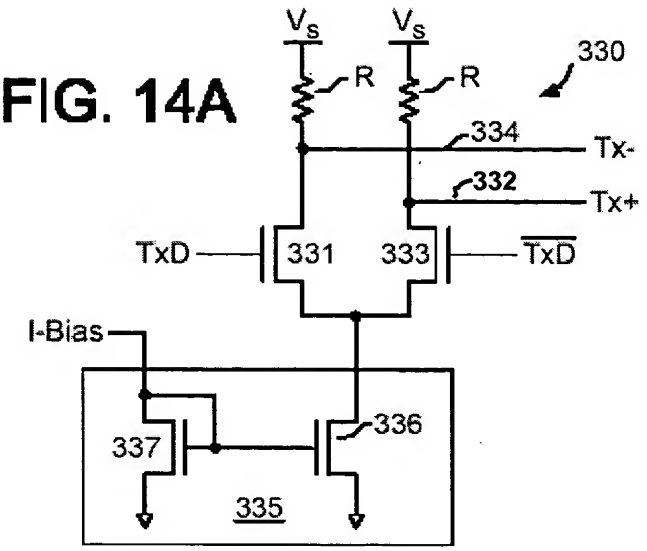

FIGURE 14A

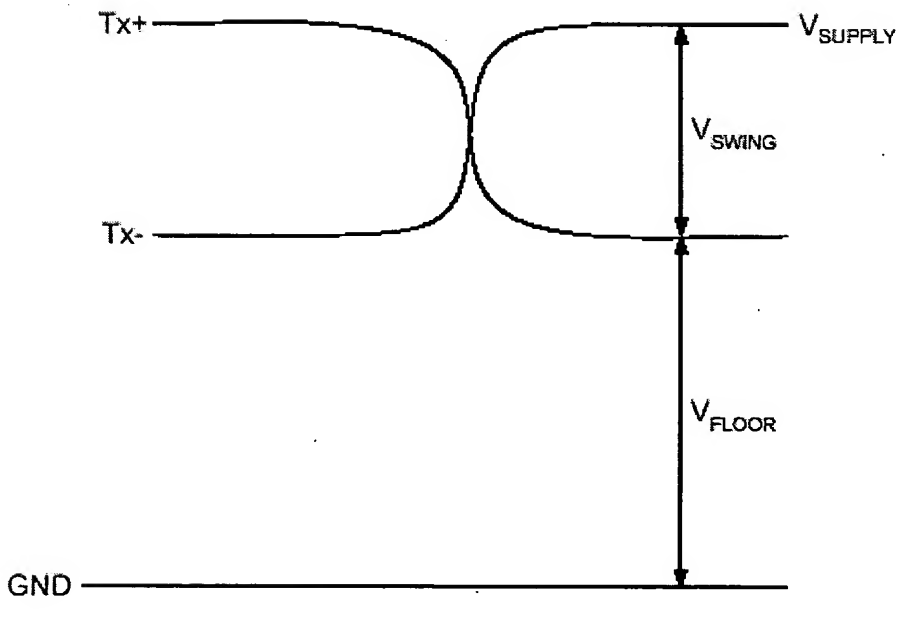

FIGURE 14B

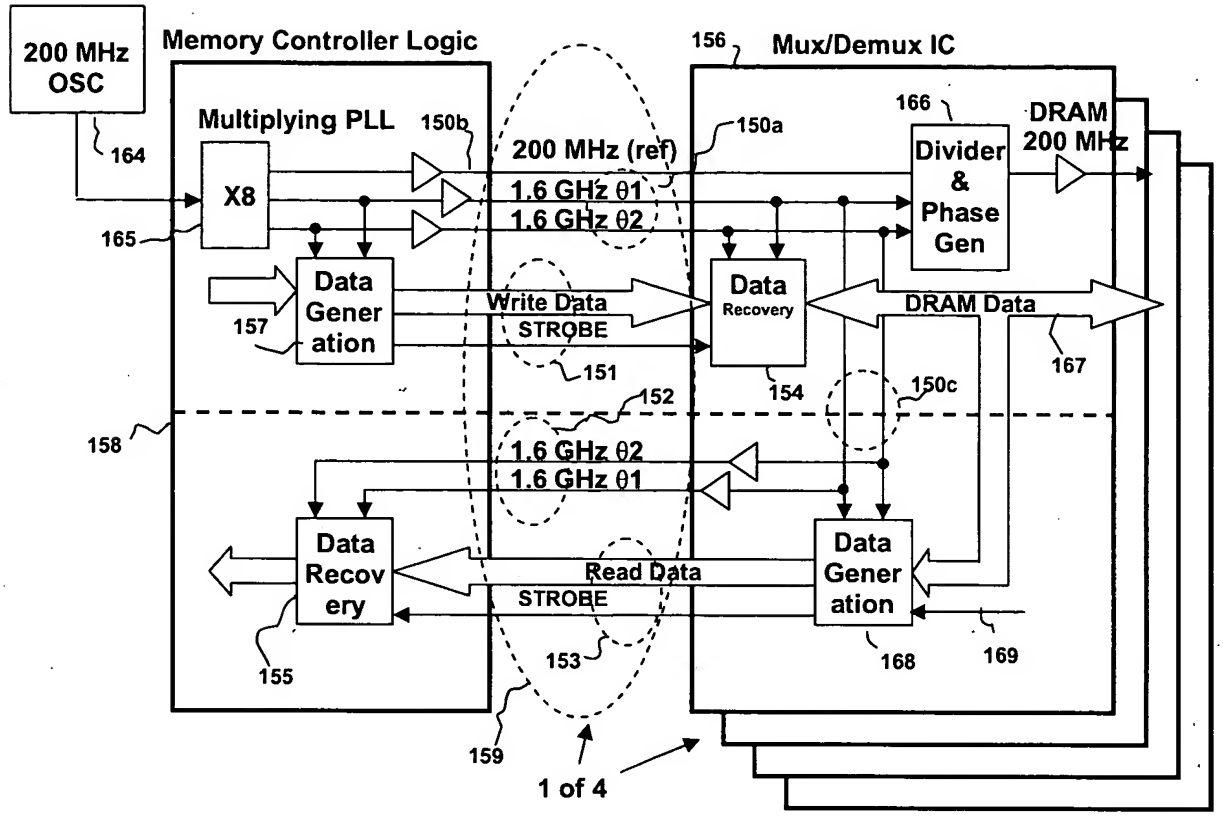

FIGURE 15

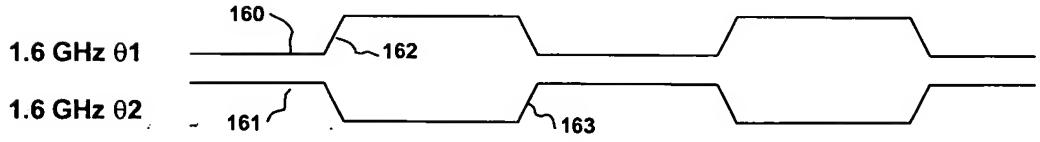

FIGURE 16

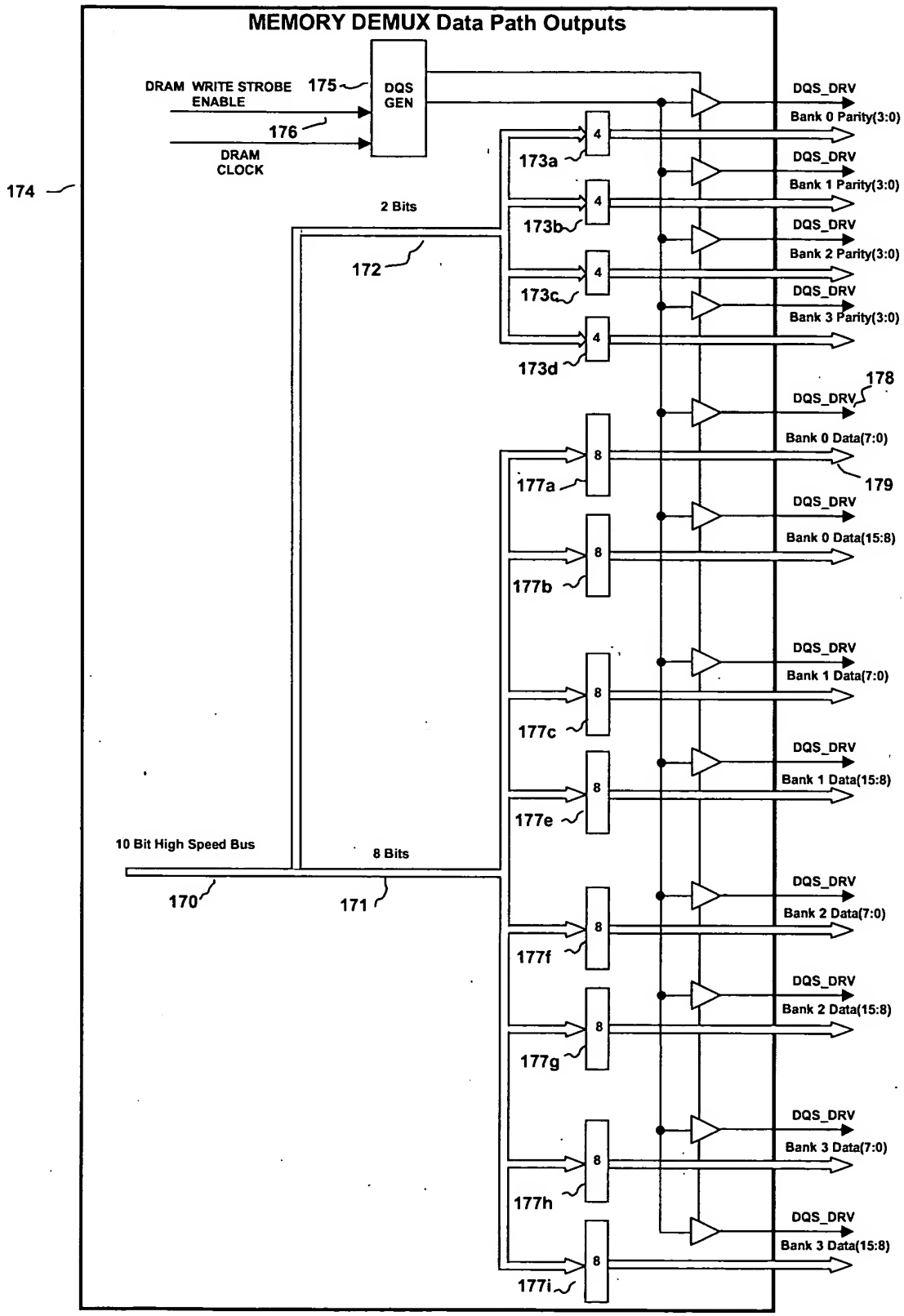
MEMORY DEMUX Data Path Outputs
DRAM WRITE STROBE ENABLE
175
DQS GEN
176
DRAM CLOCK
174
2 Bits
172
173a
173b
173c
173d
4
DQS_DRV
Bank 0 Parity(3:0)
Bank 1 Parity(3:0)
Bank 2 Parity(3:0)
Bank 3 Parity(3:0)
178
Bank 0 Data(7:0)
179
Bank 0 Data(15:8)
Bank 1 Data(7:0)
Bank 1 Data(15:8)
Bank 2 Data(7:0)
Bank 2 Data(15:8)
Bank 3 Data(7:0)
Bank 3 Data(15:8)
177a
177b
177c
177e
177f
177g
177h
177i
8
10 Bit High Speed Bus
8 Bits
170
171

FIGURE 17

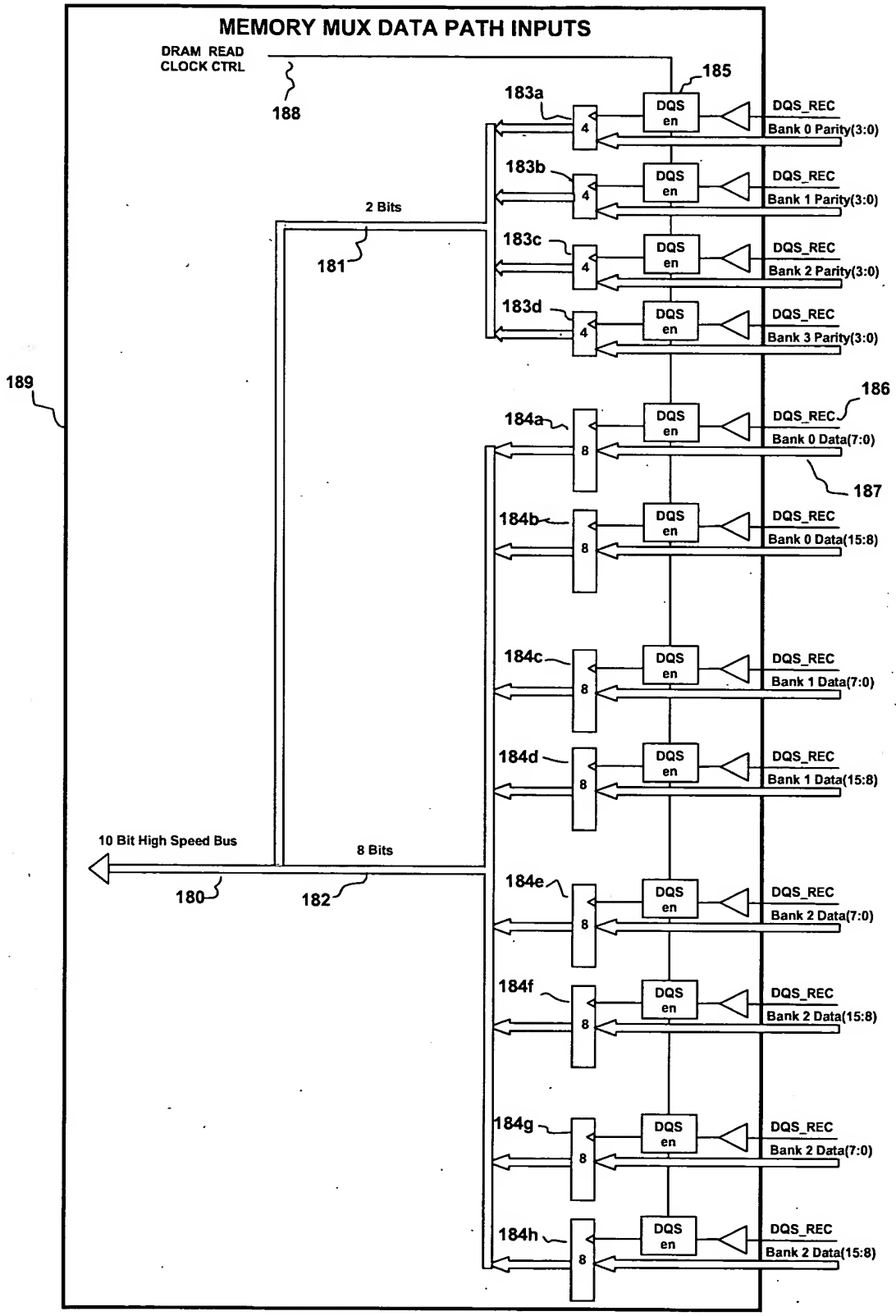
MEMORY MUX DATA PATH INPUTS
DRAM READ CLOCK CTRL
188
185
183a
183b
183c
183d
DQS en
4
DQS_REC
Bank 0 Parity(3:0)
Bank 1 Parity(3:0)
Bank 2 Parity(3:0)
Bank 3 Parity(3:0)
2 Bits
181
189
186
184a
184b
184c
184d
184e
184f
184g
184h
8
Bank 0 Data(7:0)
Bank 0 Data(15:8)
Bank 1 Data(7:0)
Bank 1 Data(15:8)
Bank 2 Data(7:0)
Bank 2 Data(15:8)
187
10 Bit High Speed Bus
8 Bits
180
182

FIGURE 18

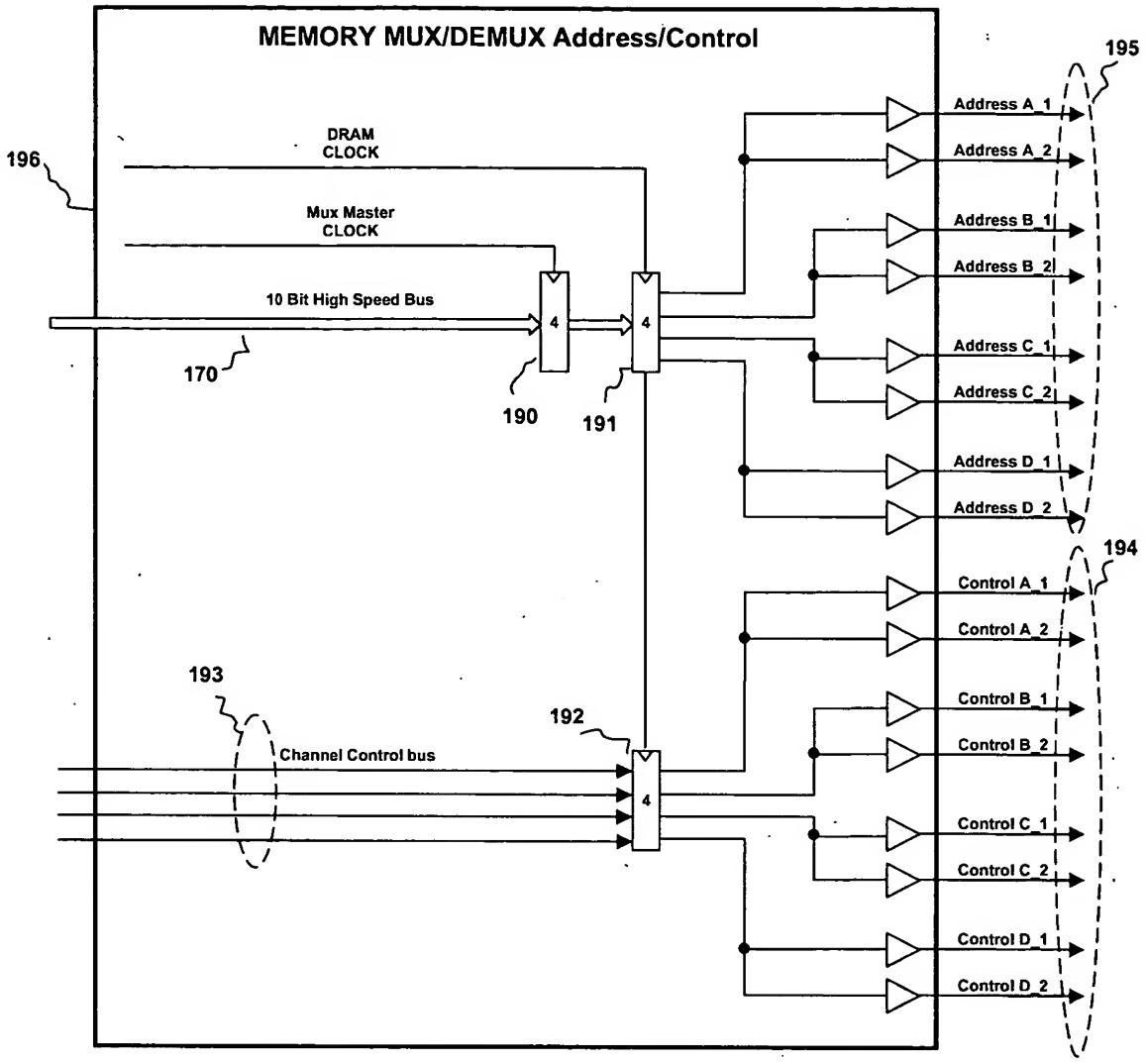
MEMORY MUX/DEMUX Address/Control
195
196
DRAM CLOCK
Mux Master CLOCK
10 Bit High Speed Bus
170
190
191
4
4
Address A_1
Address A_2
Address B_1
Address B_2
Address C_1
Address C_2
Address D_1
Address D_2
194
Control A_1
Control A_2
193
192
Channel Control bus
4
Control B_1
Control B_2
Control C_1
Control C_2
Control D_1
Control D_2

FIGURE 19

High-Speed Point-to-Point Channel Signals	Type	S or D	Pin Quan	DRAM Signals	Type	S or D	Pin Quan
Channel DATA	I/O	Dif	20	DRAM DATA	I/O	Sing	80
Channel CLK	I	Dif	2	DRAM CLOCK	O	Dif	8
Channel DESKEW CLK	O	Dif	2	DRAM REF CLK	O	Sin	2
Channel DRAM CLK	I	Dif	2	DRAM PLL CLK	I	Dif	2
Channel DIRECTION	I	Dif	2	DRAM STROBE	I/O	Sing	12
Channel STROBE ENABLE	I	Dif	2			Dif	
Channel CONTROL BUS	I	Dif	4	DRAM CONTROL	O	Sing	8
Channel Rev STROBE ENABLE	O	Dif	2	DRAM ADDRESS	O	Sing	8
		Total	**36**			**Total**	**120**

FIGURE 20